Design of Hybrid PWM Algorithm for Switched-Capacitor Multilevel Inverter Based on TMS320F28335

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Abstract –In this paper, the principle of the 7-level switched-capacitor inverter with an improved hybrid PWM strategy is presented. It only needs three carrier signals and one reference signal to synthesize output voltage, making the implementation more simplified. After that, the hardware design process is described in terms of control circuit based on TMS320F28335 floating-point digital signal processor, drive circuit and acquisition circuit. Moreover, the software design process involved in symmetrical regular sampling method and parameters of RMS voltage closed-loop control is also given in detail. Finally, the experimental results demonstrate the feasibility and high performance of the hybrid PWM strategy controlled by DSP TMS320F28335.

Keywords – Switched capacitor, multilevel inverter, TMS320F28335, hybrid PWM algorithm

I. INTRODUCTION

With many advantages of reduced dv/dt stresses, staircase output voltage waveforms and operating with lower switching frequency etc., multilevel inverters (MLI) have gradually become an important electric equipment for DC to AC power conversion in various fields [1]-[3]. Conventional MLIs are divided into three categories: neutral-point-clamped (NPC), flying capacitor (FC) and cascaded H-bridge (CHB). Nowadays, NPC and FC inverters have been successfully commercialized in many applications like FACTS [4], [5]. However, both of them have a common problem with using numerous clamping components to provide more output levels. In contrast, multiple isolated dc sources employed in CHB inverter can also generate more output levels, making the components reduced [6].

A common feature of these conventional MLIs has no boosting ability, so they need to connect the front-end boost circuit or transformer. In recent years, switched-capacitor (SC) MLIs have attracted more attention due to its boosting ability and self-balanced capacitor's voltages [7]-[9]. For instance, the conventional series/parallel SC circuit with single source invented by Hinago *et al.* in 2012 is capable of generating 2n+3 output levels [7], wherein n is the number of SC units. After that, many improved SC-MLIs are developed in the works, which can also generate 2n+3 output levels and have their own advantages [10]-[13]. In addition, since researchers focus on simpler structure to generate more output levels, some novel SC-MLIs are developed in the works [14]-[17]. The topology presented in [14] only involves eight transistors, two diodes and two capacitors, which can generate 7-level output voltage with triple boosting factor. As for [15]-[17], only 18 components employed in these 13-level topologies and they have six times boosting factor, making them suitable for low-voltage applications, such as motor control.

There are various modulation strategies adopted for SC-MLIs, such as near level control (NLC), the selective harmonic eliminated (SHE) and sinusoidal pulse width modulation (SPWM). The NLC is the simplest strategy and only suitable for more output levels. The SHE strategy can accurately reduce low-order harmonics but it needs to solve numerous nonlinear equations. In addition, SPWM strategy is to synthesize the output voltage by combining multi-carrier signals and sinusoidal reference signal, which makes the harmonics voltage concentrated near the inter multiples of switching frequency. Hence, the high-order harmonics can be suppressed by connecting a smaller LC filter with the load. Although the conventional SPWM strategies like level-shifted PWM (LS-PWM) and phase-shifted PWM (PS-PWM) can improve power quality, the capacitors' voltage ripple will accumulate when the capacitors discharges to the load continuously. In order to optimize the capacitors' voltage ripple, a hybrid PWM strategy combining LS-PWM and PS-PWM is adopted in the works [14], [15], making the voltage ripples of capacitors reduced effectively. Therefore smaller capacitors employed in these inverters can further improve power density.

In this paper, an improved hybrid PWM strategy is adopted to modulate the 7-level inverter proposed in [14]. Compared with the modulation strategy of [14] using four carriers, the improved hybrid PWM strategy only uses three ePWM modules of DSP to generate three carriers. So, it is more suitable for engineering applications. The proposed topology and PWM algorithm are described in Section II. After that, the implementation process of hybrid PWM algorithm based on TMS320F28335 is given in Section III. The experimental results verified the feasibility of the design in Section IV. Finally, the conclusion of this work gives in Section V.

II. TOPOLOGY AND MODULATION STRATEGY

A. Topology description

As shown in Fig. 1, the proposed inverter consists of an input dc source, a triple-mode SC unit and an inverting H-bridge S_3, S'_3, S_4, S'_4 to convert DC bus voltage V_{bus} to AC output voltage u_O. The triple-mode SC unit involves a pair of diodes D_1-D_2, a pair of capacitors C_1-C_2 and two pairs of transistors S_1-S_1', S_2-S_2'. By controlling these transistors reasonably, both C_1 and C_2 can be connected in series with the input dc source and charged to V_{dc}, respectively. They can also discharge to the load when connecting in parallel with the input dc source. So the V_{bus} has three different dc-levels that are $+V_{dc}$, $+2V_{dc}$ and $+3V_{dc}$. With the back-end H-bridge to alternate the output polarity, the proposed inverter is capable of generating 7-level output voltages that are 0, $\pm V_{dc}$, $\pm 2V_{dc}$ and $\pm 3V_{dc}$.

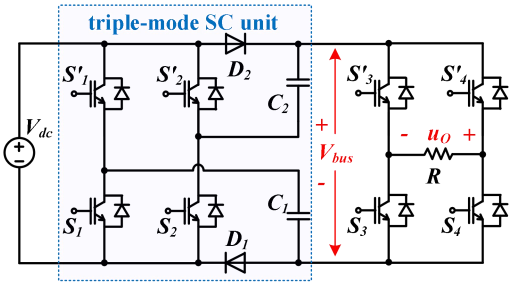

Fig.1: 7-level inverter proposed in [14].

B. Operation principle

To facilitate the analysis, the operating states of the zero and half-positive output levels are indicated in Fig. 2.

(i) State 1(u_O=+3V_{dc}): As shown in Fig. 2(a), in this operating state, the capacitors C_1 and C_2 are connected in series with the input dc source to power the load through S_1, S'_2, S_3 and S'_4. The output level is therefore +3V_{dc}.

(ii) State 2(u_O=+2V_{dc}): As shown in Fig. 2(b), the capacitors C_2 is charged to V_{dc} by the dc source through S_1 and D_2, while C_1 is connected in series with the dc source to power the load through S_1, S_3, S'_4 and D_2. In addition, as shown in Fig. 2(c), the capacitors C_1 is charged to V_{dc} by the dc source through S'_1 and D_1, while C_2 is connected in series with the dc source to power the load through S'_2, S_3, S'_4 and D_1. Therefore, the output level of Fig. 2(b) and (c) is therefore +2V_{dc}.

(iii) State 3 (u_O=+V_{dc}): As shown in Fig. 2(d), both capacitors C_1 and C_2 and dc source are connected in parallel then they are charged to V_{dc}, simultaneously. The dc source discharges to the load directly so that the output level is +V_{dc}.

(iv) State 4 (u_O=0): In this state, the transistors S_3 and S_4 or the transistors S'_3 and S'_4 are turned ON, making the zero output level generated as shown in Fig. 2(e) and (f), respectively. In addition, Both C_1 and C_2 are still charged by the dc source.

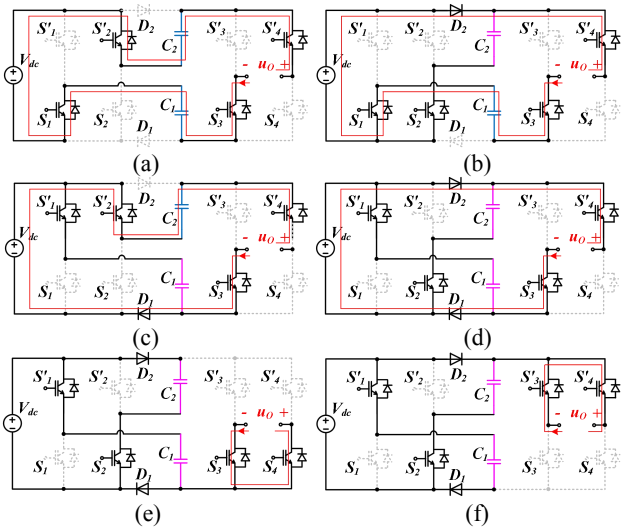

Fig.2: Operating states of zero and half-positive output levels. (a) u_O=+3V_{dc}. (b) and (c) u_O=+2V_{dc}. (c) u_O=+V_{dc}. (e) and (f) u_O=0.

By alternating the polarity of back-end H-bridge, the negative output levels are generated with the same operating states of triple-mode SC unit. Table 1 shows the operating states during one output cycle. Note that "1" and "0" represent "ON" and "OFF", respectively, while capacitors' states are noted by "▼"and "▲", which represent as discharging and charging states, respectively.

Table 1: Operating states of the proposed inverter during one output cycle

State	Capacitor's states		Switching states				u_O
	C_1	C_2	S_1	S_2	S_3	S_4	
1	▼	▼	1	0	1	0	+3V_{dc}
2	▼	▲	1	1	1	0	+2V_{dc}
	▲	▼	0	0	1	0	
3	▲	▲	0	1	1	0	+V_{dc}
4	▲	▲	0	1	0	0	0
	▲	▲	0	1	1	1	
5	▲	▲	0	1	0	1	-V_{dc}
6	▲	▼	0	0	0	1	-2V_{dc}
	▼	▲	1	1	0	1	
7	▼	▼	1	0	0	1	-3V_{dc}

C. Hybrid PWM strategy

As shown in Table 1, there are two switching states when the output levels are ±2V_{dc}, respectively. One of the capacitor is charged by the dc source, while the other discharges to the load. Taking the operating states of the half-positive cycle as an example, Fig. 3 illustrates the charging and discharging process of two capacitors between the +2V_{dc} and +3V_{dc}. It indicates that C_1 is charged from 0 to t_1 and discharges to the load from t_1 to t_2, continuously. And then it charged by the dc source again. The capacitor C_2 has the same feature as C_1. Due to its redundant states, two capacitors can be alternately charged by the dc source, making their voltage ripples reduced.

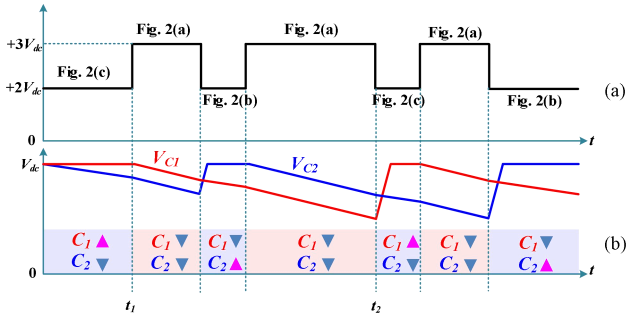

Fig.3: Operating states between +2V_{dc} and +3V_{dc} with hybrid PWM. (a) Output levels. (b) Capacitors' states.

Considering the feature of the proposed inverter, a hybrid PWM strategy combining LS-PWM and PS-PWM is adopted to modulate the proposed inverter. As shown in Fig. 4(a), all gate signals are generated by using three carrier signals u_1-u_3 and one sinusoidal reference signal u_r, where the amplitude of u_1 and u_2 is 2A_C, that of u_3 is A_C, and that of u_r is A_R. Therefore, the modulation ratio M_a can be given by

$$M_a = \frac{A_R}{3A_c} \quad (1)$$

To ensure the generation of 7-level output voltage, M_a have to satisfy the condition, i.e.

$$1 \geq M_a \geq \frac{2}{3} \quad (2)$$

Fig. 4(b) illustrates the logic circuit with the hybrid modulation. It shows that the absolute value of u_r are used to compare with u_1-u_3 for generating their original pulse

signals, while the polarity of u_r is determined by comparing with zero potential point. Combining three original pulse signals and the polarity of u_r, four gate signals V_{GS1}-V_{GS4} for eight transistors are generated.

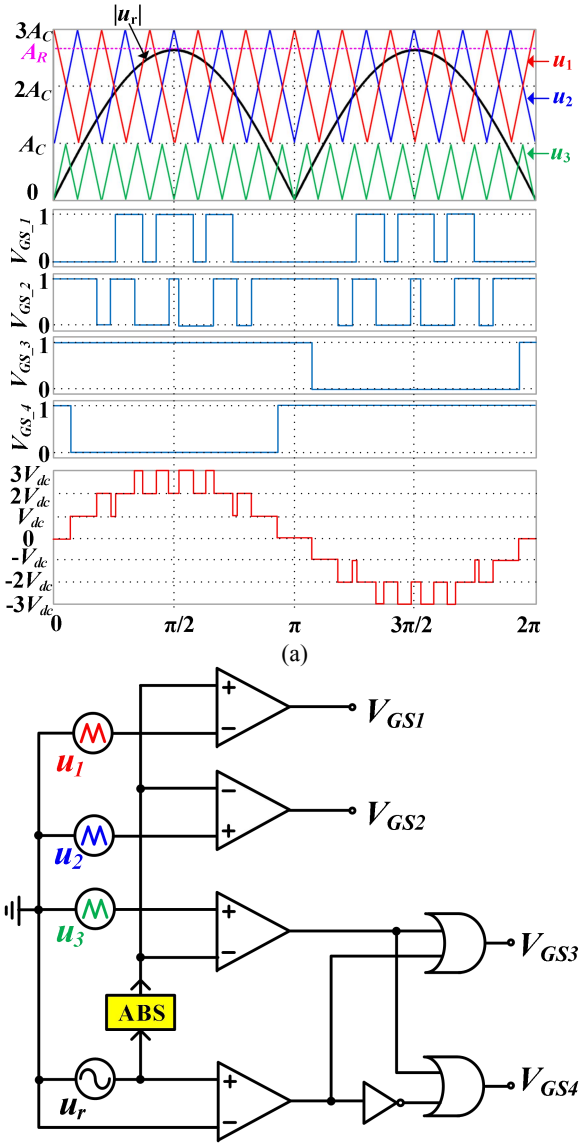

Fig.4: The proposed inverter with hybrid PWM modulation. (a) Waveforms. (b) Logic circuit of modulation.

III. Implementation Based on DSP Controller

There are many types of processors to control the switching states of the proposed inverter, such as microcontroller unit, field-programmable gate array and digital signal processor (DSP). Among them, the TMS320F28335 floating-point DSP is good at computing and generating high-frequency PWM signals. So it is adopted to implement the hybrid PWM algorithm.

As shown in Fig. 5, the system structure consists of DSP circuit, drive circuit, acquisition circuit and inverter circuit. The PWM signals generated from the DSP are amplified by the drive circuit to control the transistors of the inverter. In addition, the instantaneous output voltage measured by acquisition circuit is used for calculating the RMS of output voltage. So it can realize the RMS voltage closed-loop control by adjusting the modulation ratio.

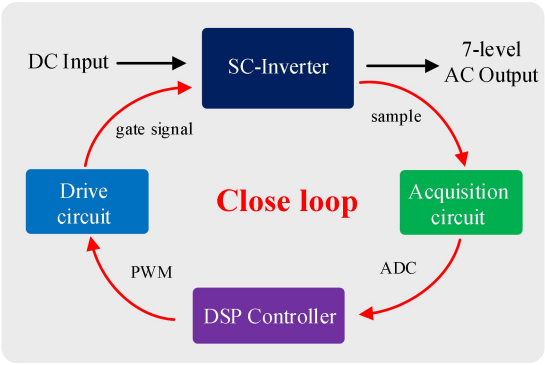

Fig.5: Control system structure.

A. DSP circuit

To implement the hybrid PWM strategy, the DSP core-board based on TMS320F28335 have been designed as shown in Fig. 6. The power supply system is composed of two low-dropout regulators that are used to convert 5V input voltage to 3.3V and 1.9V output voltages for the inner power and external power of the TMS320F28335, respectively. Since DSP TMS320F28335 has floating-point units and its main frequency is up to 150MHz, the processing speed is so fast that the ePWM module can generate high-frequency PWM signals. In addition, four 12-bit ADC modules integrated in DSP are used to convert the analog signal to the digital signal that can be processed by DSP. Normally, there are many factors that can interfere with analog signals, such as voltage spike, inrush current and switching noise. In order to protect the ADC modules, low-pass filters and surge suppression circuits are designed in this core-board.

Fig.6: DSP core-board based on TMS320F28335.

B. Drive circuit

There are two H-bridges employed in the proposed inverter as shown in Fig. 1. Therefore, the drive circuit uses IR2111 to generate both complementary gate signals with internal deadtime. Due to the IR2111 supply range from 10V to 20V, the logic input voltage is beyond the 3.3V LVTTL. To match the logic level and protect the core-board, high-speed optocouplers TLP251 are also designed in this circuit. Fig. 7 shows its schematic diagram.

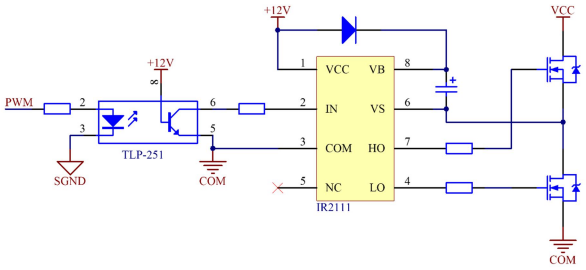

Fig.7: Schematic diagram of drive circuit.

C. Acquisition circuit

To measure instantaneous output voltage accurately, the hall-effect voltage sensor VSM025A is employed in the acquisition circuit. Since the voltage sensor requires positive-negative power and its measured signal is proportional to the output voltage, the dc-bias circuit must be adopted to make the voltage of measured analog signal between 0V and 3.3V. And therefore ADC module converts it to digital signal, correctly. The schematic diagram of acquisition circuit is shown in Fig. 8.

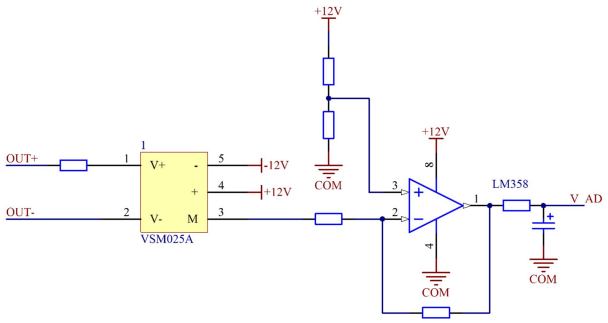

Fig.8: Schematic diagram of acquisition circuit.

D. Software design

To implement hybrid PWM algorithm in software design, the ePWM module, ADC module and PI module in DSP are programming with CCSv8. Specifically, the design process is summarized as follow steps:

Step 1: Due to less computation, symmetrical regular sampling method has been widely used for generating SPWM waveforms. It samples the amplitude of reference signal at the vertices or lowest points of the triangular carrier signal. Fig. 9 illustrates the principle of sampling process.

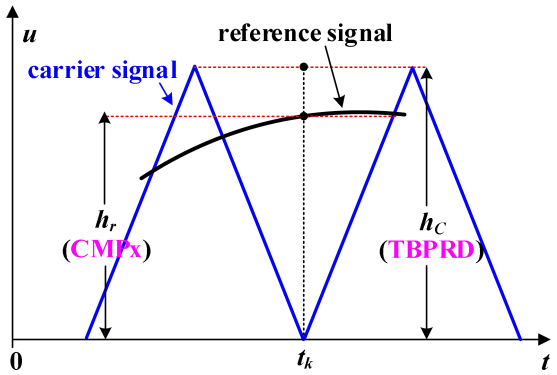

Fig.9: The principle of symmetrical regular sampling method.

At the *kth* sampling moment, it can be seen that the amplitude of carrier signal is h_C and that of reference signal is h_r. In addition, the continuous up down mode of the ePWM module gives the same symmetric carrier waveform and the TBPRD register value is proportional to h_C. Similarly, the CMPx register value is also proportional to h_r and it can therefore be calculated by

$$CMPx = \frac{h_r}{h_c} \times TBPRD \tag{3}$$

To make the SPWM more accurate, the frequency of carrier signal must be much larger than that of reference one. Assuming that there are N_C carrier signals during one cycle of reference signal, the number of sampling values calculated from (3) is also N_C. As mentioned before, three carrier signals u_1-u_3 are used for generating original PWM signals, where u_1 and u_2 have the same frequency but the their phase difference is 180°, while the frequency of u_3 is double of them. By setting three ePWM modules, three groups of sampling values can be obtained.

Step 2: After calculating three groups of sampling values, the CMPx register value can be updated to sampling values in the interruption procedure caused by ePWM event and then three original PWM signals are generated. Except for gate signals V_{GS1} and V_{GS2}, the remaining gate signals are synthesized through logic operations as shown in Fig. 4(b).

Step 3: As mentioned before, the RMS value of output voltage is proportional to the modulation ratio M_a. So the target value of RMS voltage can be determined by that of M_a. To realize the RMS voltage closed-loop control, the acquisition circuit needs to measure N_C instantaneous values to calculate the measured RMS value during one output cycle, i.e.

$$V_{RMS} = \sqrt{\frac{\left(V_i - \frac{1}{N_C}\sum_{i=1}^{N_C} V_i\right)^2}{N_C}} \tag{4}$$

After that, digital PI module is employed to adjust the M_a by comparing the difference between target values and measured values. Its discrete expression can be given as

$$u(k) = u(k-1) + \left(K_p + \frac{TK_p}{T_i}\right)e(k) - K_p e(k-1) \tag{5}$$

where sample time T is consistent with time interval of interruption procedure triggered by ePWM events. In addition, the modulation ratio M_a calculated by the digital PI module is to control RMS value of output voltage during one output cycle.

To simplify the analysis, the overall flow chart of software design is shown in Fig. 10.

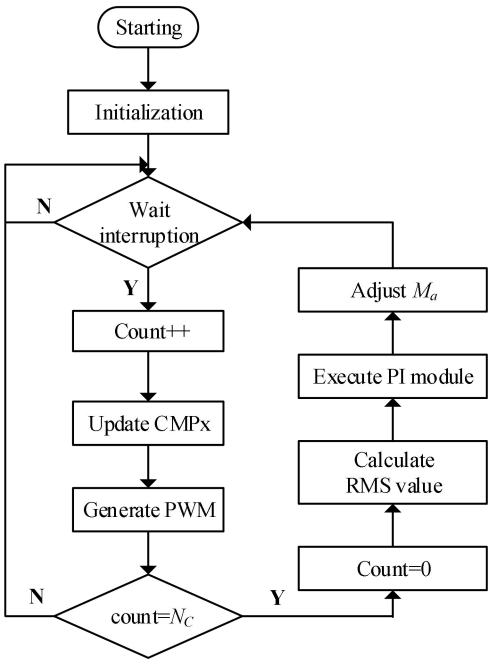

Fig.10: Flow chart of software design.

IV. Experimental Results

To verify the feasibility and high performance of the proposed inverter with hybrid modulation strategy, a 80W

experimental prototype was built by referring its specification and components in Table 2.

Table 2: Specification and components of the 7-level prototype

Input dc voltage	50VDC
Rated power	80W
Output voltage's frequency	50Hz
Switching frequency	5kHz
Capacitors C_1,C_2	1000μF
Transistors S_1,S_1',S_2,S_2'	IRFB4410PBF
Transistors S_3,S_3',S_4,S_4'	IRFB4229PBF
Half-bridge driver IC	IR2111
High-speed optocoupler	TLP251
Controller	TMS320F28335

When the M_a is set to 0.87, four gate signals for eight transistors are shown in Fig. 11, which is corresponding to the analysis in Fig. 4(a). With an inductive load 100Ω-53mH, it can also be seen that the output voltage u_O is the high-frequency seven-level SPWM waveform, while the output current i_O is very closed to sinusoidal waveform. In addition, as u_O is switched quickly between $+2V_{dc}$ and $+3V_{dc}$, the voltage of two capacitors are alternatively replenished by the dc source. Similarly, they also have the same behavior when u_O is switched quickly between $-2V_{dc}$ and $-3V_{dc}$. Therefore, two capacitors can be balanced automatically and their voltages' ripples can be reduced effectively.

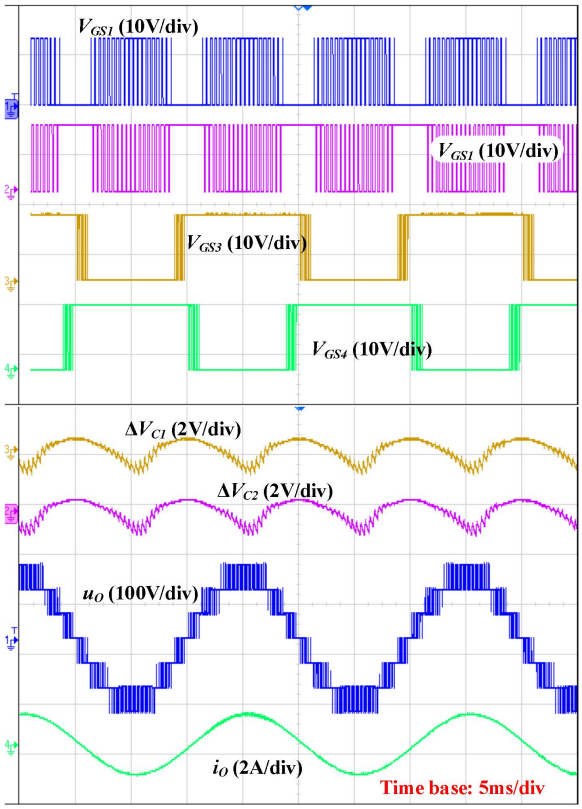

Fig.11: Experimental waveforms of an inductive load 100Ω–53mH.

To further verify the effect of reducing harmonics with the hybrid PWM algorithm, FFT analysis results in respect of output voltage and current are given in Fig. 12. It illustrates that the low-order harmonics of output voltage have been reduced by concentrating the harmonics around an integer multiple of the switching frequency. Therefore, a smaller LC filter is used for filtering out high-order harmonics. For the output current, the harmonics have been suppressed effectively by the inductive load, where the amplitude of maximum harmonics is only 7mA.

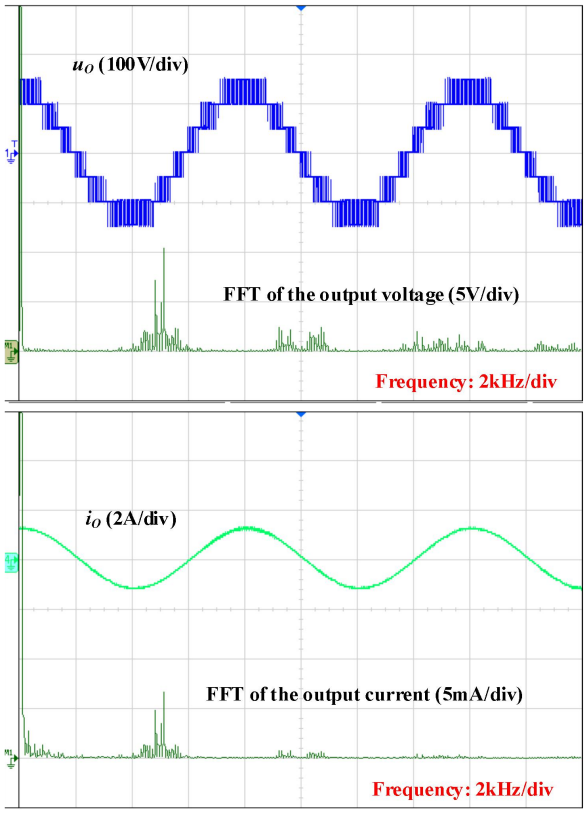

Fig.12: FFT analysis results of the output voltage and current.

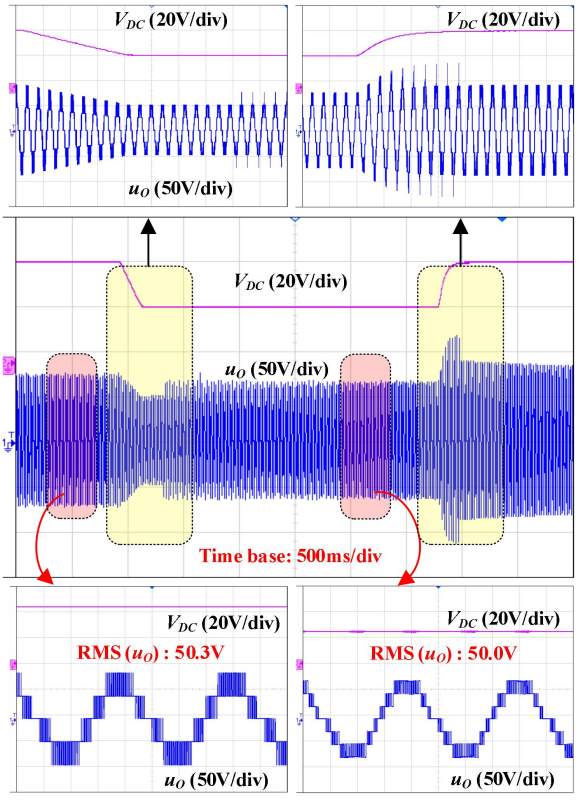

Fig.13: Experimental waveforms when the input dc voltage changes between 25V and 45V.

Fig. 13 illustrates the dynamic performance of RMS output voltage closed-loop control. Specifically, the target value of RMS voltage, K_p and T_i are set to 50V, 0.025 and 0.0075, respectively. When the input dc voltage is suddenly changed from 45V to 25V, the RMS voltage reduces accordingly but it quickly returns to the measured value 50.3V by increasing the modulation ratio M_a and remains stable. And then when the input dc voltage changes back to 45V, the RMS voltage also increases suddenly and it quickly returns to the measured value 50.0V by reducing the modulation ratio M_a. Therefore, it demonstrates that the closed-loop control for RMS output voltage has good adaptive adjustment ability.

V. Conclusion

This work analyzes the operating principle of the proposed SC-MLI with the improved hybrid PWM algorithm. With this modulation strategy, the voltages' ripples of two capacitors can be optimized, making the power density increase. In addition, the control board based on DSP TMS320F28335 is designed for implementing PWM algorithm and RMS voltage closed-loop control. The design of drive circuit, acquisition circuit and software programming is also discussed in detail. The experimental results demonstrate that the voltages' ripples of capacitors can be reduced effectively with the hybrid PWM algorithm and the digital PI controller can improve the dynamic performance.

Acknowledgment

The authors appreciate the financial support of the National Nature Science Foundation of China under the project number 51907033.

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